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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,854	09/30/2003	Lester J. Kozlowski	354096.01300	6861

58076 7590 05/17/2006

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EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,854	KOZLOWSKI, LESTER J.	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/30/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claim 11 is objected to because of the following informalities:

Claim 11 (lines 2-3), "the improvement" should be changed to --an improvement--.

Claim 11 (line 3), "an access supply connected to a column bus" should be changed to -- an access supply connected to a row bus--. Noted that the specification, page 7 indicates that "row bus 220 connects all pixel resets in a row to an access supply 400.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozlowski et al. (US 6,493,030).

Regarding claim 1, Kozlowski et al. discloses a pixel circuit comprising:

a photodetector (photodetector 12, figure 4, column 5, lines 35-65) connected to a first node (the node connects cathode of photodetector 12 to the gate of MOSFET 14, figure 4);

a dual-driver MOSFET having a gate connected to the first node (dual-driver MOSFET 14, figure 4);

a reset MOSFET (reset MOSFET 16, figure 4, column 5, lines 35-65) having a first leg connected to the first node and a second leg connected to a second node (the node connects one leg of reset MOSFET 16 to one leg of dual-driver MOSFET 14, figure 4, column 5, lines 35-65);

an access MOSFET (MOSFET 20, figure 4, column 5, lines 35-65) having a first leg connected to a row bus and a second leg connected to the second node;

a row select MOSFET (row select MOSFET 18, figure 4, column 5, lines 35-65) having a first leg connected to the dual-driver MOSFET and a second leg connected to a column bus (column bus 24, figure 4);

an access supply connected to the row bus (access supply Vdd, figure 4, column 5, lines 35-65);

a source supply connected to the column bus (source power supply 30, figure 4, column 5, lines 35-65);

a reset supply connected to a gate of the reset MOSFET (tapered reset supply 50, figure 4, column 5, lines 35-65);

wherein the MOSFETs all have the same polarity (figure 4 shows that the MOSFETs 14, 16, 18, 20, all have the same polarity).

Regarding claim 2, Kozlowski et al. discloses wherein the photodetector is a photodiode (photodiode 12, figure 4, column 5, lines 35-65.

Regarding claim 3, Kozlowski et al. discloses wherein the access supply comprises a current source that is a distributed feedback amplifier when connected to the MOSFETs (figure 7, column 6, lines 35-54).

Regarding claim 4, Kozlowski et al. discloses wherein wherein the feedback amplifier (feedback amplifier 44, figure 7, column 6, lines 35-54) is a cascaded inverter.

Regarding claim 5, Kozlowski et al. discloses wherein the reset supply produces a tapered waveform (tapered reset supply 50, figures 4, 9, column 5, lines 35-57).

Regarding claim 6, Kozlowski et al. discloses operational amplifier (amplifier 44, figure 7), a bias transistor (transistor 48, figure 7) and a mode transistor (transistor 46, figure 7).

Regarding claim 7, Kozlowski et al. discloses wherein the MOSFETs are N-type MOSFETs (figure 4 shows that the MOSFETs 14, 16, 18, 20 N-type MOSFETs).

Regarding claim 8, Kozlowski et al. discloses an active pixel having a plurality of pixel sensors (sensor array, column 5, lines 35-40), each pixel sensor comprising:

a photodiode (photodetector 12, figure 4, column 5, lines 35-65) connected to a first node (the node connects cathode of photodetector 12 to the gate of MOSFET 14, figure 4);

a dual-driver MOSFET having a gate connected to the first node (dual-driver MOSFET 14, figure 4);

a reset MOSFET (reset MOSFET 16, figure 4, column 5, lines 35-65) having a first leg connected to the first node and a second leg connected to a second node (the node connects one leg of reset MOSFET 16 to one leg of dual-driver MOSFET 14, figure 4, column 5, lines 35-65);

an access MOSFET (MOSFET 20, figure 4, column 5, lines 35-65) having a first leg connected to a row bus and a second leg connected to the second node;

a row select MOSFET (row select MOSFET 18, figure 4, column 5, lines 35-65) having a first leg connected to the dual-driver MOSFET and a second leg connected to a column bus (column bus 24, figure 4);

an access supply connected to the row bus (access supply Vdd, figure 4, column 5, lines 35-65), the access supply comprising a distributed feedback amplifier (feedback amplifier 44, figure 7, column 6, lines 35-54);

a source supply connected to the column bus (source power supply 30, figure 4, column 5, lines 35-65);

a reset supply connected to a gate of the reset MOSFET (tapered reset supply 50, figure 4, column 5, lines 35-65), the reset supply producing a tapered reset waveform (column 5, lines 45-50, figures 4, 9);

wherein the MOSFETs all have the same polarity (figure 4 shows that the MOSFETs 14, 16, 18, 20, all have the same polarity).

Regarding claim 9, Kozlowski et al. discloses an operational amplifier (amplifier 44, figure 7), a bias transistor (transistor 48, figure 7) and a mode transistor (transistor 46, figure 7).

Regarding claim 10, Kozlowski et al. discloses wherein the MOSFETS are N-type MOSFETs (figure 4 shows that the MOSFETs 14, 16, 18, 20 N-type MOSFETs).

Regarding claim 11, all the limitations are contained in claim 8. Therefore, see Examiner's comments regarding claim 8.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Denyer et al. (US 5,926,214) discloses camera system and associated method for removing reset noise and fixed offset noise from the output of an active pixel array.

Kozlowski et al. (US 6,697,111) discloses compact low-noise active pixel sensor with progressive row reset.

Zhao et al. (US 6,727,946) discloses APS soft reset circuit for reducing image lag.

Bencuya et al. (US 6,911,640) discloses reducing reset noise in CMOS image sensors.

Dierickx (US 2001/0045508) discloses pixel structure for imaging devices.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
05/15/06

Luonahuna Nguyen

LUONG T. NGUYEN
PATENT EXAMINER